In the Claims

1-37 (Cancelled)

38 (New): A control circuit for an input/output terminal of an integrated circuit comprising:

a first voltage detection circuit having an input for receiving a first supply voltage signal and an output for providing a first detection signal that indicates when the voltage level of the first supply voltage signal is below a first steady state supply level;

a second voltage detection circuit having an input for receiving a second supply voltage signal and an output for providing a second detection signal that indicates when the voltage level of the second supply voltage signal is below a second steady state supply level; and

a logic circuit for receiving the first and second detection signals and providing at least one detected condition signal for disabling current flow through the input/output terminal when either the first supply voltage signal is below the first steady state supply level or the second supply voltage signal is below the second steady state supply level;

a first pull-up transistor having a source and a drain connected between the input/output terminal and a first pull-up supply voltage signal;

a first pull-down transistor having a source and a drain connected between the input/output terminal and a first pull-down supply voltage signal,

a second pull-up transistor having a source and a drain connected between a gate of the first pull-up transistor and a second pull-up supply voltage signal; and

a second pull-down transistor having a source and a drain connected between a gate of the first pull-down transistor and a second pull-down supply voltage signal,

wherein a detected condition signal is applied to a gate of the second pull-up transistor and to a gate of the second pull-down transistor.

39 (New): The control circuit of claim 38 wherein the first pull-up supply voltage signal and the second pull-up supply voltage signal are the same.

40 (New): The control circuit of claim 38 wherein the first pull-down supply voltage signal and the second pull-down supply voltage signal are the same.

41 (New): The control circuit of claim 38 wherein the logic circuit provides a first detected condition signal that is applied to the gate of the second pull-up transistor and a second detected condition signal, complementary to the first detected condition signal, that is applied to the gate of the second pull-down transistor.

42. (New): The detection circuit of claim 38 wherein each of the first and second voltage detection circuits comprises:

a first latch having an input and an output, the output of said voltage detection circuit being at the input of the first latch;

a first transistor coupled between the input of said voltage detection circuit and the output of the first latch, the first transistor having a control terminal coupled to a node for a power signal for said voltage detection circuit; and

a second transistor coupled between a reference supply voltage and the input of the first latch, the second transistor having a control terminal coupled to the input of said voltage detection circuit.

43 (New): The detection circuit of claim 42 wherein the first transistor has a lower conductivity than the second transistor.

44 (New): The detection circuit of claim 43 wherein the first steady state supply level is greater than or equal to the second steady state supply level, the power signal for the first voltage detection circuit is the greater of the first supply voltage signal and a signal corresponding to the voltage at the input/output terminal, and the power signal for the second voltage detection circuit is the first supply voltage signal.

45 (New): The detection circuit of claim 43 wherein the first steady state supply level is greater than or equal to the second steady state supply level, and the power signal for each of the first and second voltage detection circuits is the greater of the first supply voltage signal and a signal corresponding to the voltage at the input/output terminal.

46 (New): The detection circuit of claim 43 wherein

the first transistor is an NMOS transistor having a source terminal coupled to the input of said voltage detection circuit, a drain terminal coupled to the output of the first latch, and a gate terminal coupled to the power signal node for said voltage detection circuit; and

the second transistor is an NMOS transistor having a source terminal coupled to the reference supply voltage, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the input of said voltage detection circuit.

47 (New): The detection circuit of claim 43 wherein the first latch is a half latch comprising:

an inverter having an input and an output, the input of the inverter being the input of the first latch and the output of the inverter being the output of the first latch; and

a third transistor coupled between the input of the first latch and the power signal node for said voltage detection circuit, the third transistor having a control terminal coupled to the output of the first latch.

48 (New): The detection circuit of claim 47 wherein each of the first and second voltage detection circuits includes a second half latch comprising:

a second inverter having an input and an output, the input of the second inverter being coupled to the input of the first latch;

a fourth transistor coupled between the input of the first latch and the power signal node for said voltage detection circuit, the third transistor having a control terminal coupled to the output of the second inverter.

49 (New): The detection circuit of claim 48 wherein

the third transistor is a PMOS transistor having a source terminal coupled to the power signal node for said voltage detection circuit, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the output of the first latch; and

the fourth transistor is a PMOS transistor having a source terminal coupled to the power signal node for said voltage detection circuit, a drain terminal coupled to the input of the first latch, and a gate terminal coupled to the output of the second inverter.

50 (New): The detection circuit of claim 38 wherein the logic circuit comprises a NOR gate having a first input for receiving the first detection signal and a second input for receiving the second detection signal, and wherein the logic circuit generates a pair of complementary detected condition signals.

51 (New): The detection circuit of claim 38 wherein the integrated circuit is fabricated using CMOS technology.

52 (New): The detection circuit of claim 38 wherein the integrated circuit device is a programmable logic device.

53 (New): An integrated circuit device comprising:

a plurality of terminals including

a first power terminal for receiving an input/output supply voltage signal;

a second power terminal for receiving a core supply voltage signal; and

one or more input/output terminals for receiving input signals to the device or delivering output signals from the device; and

for each input/output terminal, a supply voltage detection circuit comprising:

a first voltage detection circuit having an input for receiving the input/output supply voltage signal and an output for providing a first detection signal that indicates when the level of the input/output supply voltage signal is below a steady state input/output supply level;

a second voltage detection circuit having an input for receiving the core supply voltage signal and an output for providing a second detection signal that indicates when the level of the core supply voltage signal is below a steady state core supply level;

a logic circuit for receiving the first and second detection signals and providing at least one detected condition signal for disabling current flow through the input or the output terminal when either the input/output supply voltage signal is below the steady state input/output supply level or the core supply voltage signal is below the steady state core supply level;

a first pull-up transistor having a source and a drain connected between the input/output terminal and a first pull-up supply voltage signal;

a first pull-down transistor having a source and a drain connected between the input/output terminal and a first pull-down supply voltage signal,

a second pull-up transistor having a source and a drain connected between a gate of the first pull-up transistor and a second pull-up supply voltage signal; and

a second pull-down transistor having a source and a drain connected between a gate of the first pull-down transistor and a second pull-down supply voltage signal,

wherein a detected condition signal is applied to a gate of the second pull-up transistor and to a gate of the second pull-down transistor.

54 (New): The control circuit of claim 53 wherein the first pull-up supply voltage signal and the second pull-up supply voltage signal are the same.

55 (New): The control circuit of claim 53 wherein the first pull-down supply voltage signal and the second pull-down supply voltage signal are the same.

56 (New): The control circuit of claim 53 wherein the logic circuit provides a first detected condition signal that is applied to the gate of the second pull-up transistor and a second detected condition signal, complementary to the first detected condition signal, that is applied to the gate of the second pull-down transistor.

57 (New): The integrated circuit device of claim 53 wherein, in each of the supply voltage detection circuits, each of the first and second voltage detection circuits comprises:

a first latch having an input and an output, the output of said voltage detection circuit being at the input of the first latch;

a first transistor coupled between the input of said voltage detection circuit and the output of the first latch, the first transistor having a control terminal coupled to a node for a power signal for said voltage detection circuit; and

a second transistor coupled between a reference supply voltage and the input of the first latch, the second transistor having a control terminal coupled to the input of said voltage detection circuit.

58 (New): The integrated circuit device of claim 57 wherein, in each of the first and second voltage detection circuits in each of the detection circuits, the first transistor has a lower conductivity than the second transistor.

59 (New): The detection circuit of claim 53 wherein the integrated circuit device is a programmable logic device.

60 (New): A circuit or an input/output terminal of an integrated circuit device, comprising:

a first power terminal for receiving a first supply voltage signal;

a second power terminal for receiving a second supply voltage signal;

a first voltage detection circuit having an input coupled to the first power terminal and an output providing a first detection signal that indicates when the voltage level of the first supply voltage signal is below a first steady state supply level;

a second voltage detection circuit having an input coupled to the second power terminal and an output providing a second detection signal that indicates when the voltage level of the second supply voltage signal is below a second steady state supply level;

a logic circuit having first and second inputs coupled respectively to the outputs of the first and second voltage detection circuits, the logic circuit having at least one output providing at least one detected condition signal that disables current flow through the input/output terminal when either the first supply voltage signal is below the first steady state supply level or the second supply voltage signal is below the second steady state supply level;

a first pull-up transistor having a source and a drain connected between the input/output terminal and a first pull-up supply voltage signal;

a first pull-down transistor having a source and a drain connected between the input/output terminal and a first pull-down supply voltage signal,

a second pull-up transistor having a source and a drain connected between a gate of the first pull-up transistor and a second pull-up supply voltage signal; and

a second pull-down transistor having a source and a drain connected between a gate of the first pull-down transistor and a second pull-down supply voltage signal,

wherein a detected condition signal is applied to a gate of the second pull-up transistor and to a gate of the second pull-down transistor.

61 (New): The control circuit of claim 60 wherein the first pull-up supply voltage signal and the second pull-up supply voltage signal are the same.

62 (New): The control circuit of claim 60 wherein the first pull-down supply voltage signal and the second pull-down supply voltage signal are the same.

63 (New): The control circuit of claim 60 wherein the logic circuit provides a first detected condition signal that is applied to the gate of the second pull-up transistor and a second detected condition signal, complementary to the first detected condition signal, that is applied to the gate of the second pull-down transistor.

64 (New): The detection circuit of claim 60 wherein the first supply voltage signal is provided by an input/output power supply coupled to the first power terminal, and the second supply voltage signal is provided by a core power supply coupled to the second power terminal.